What is claimed is:

1. A master-slave-type scanning flip-flop circuit for use in testing a semiconductor integrated circuit device, comprising:

a master latch and a slave latch each for temporarily holding an input signal;

a first scan controller for receiving an output signal from said master latch and outputting the received output signal in synchronism with a scan clock which is a clock for testing the semiconductor integrated circuit device, when the semiconductor integrated circuit device is tested;

a clock controller for receiving an output signal from said first scan controller and outputting the received output signal to said slave unit in synchronism with a predetermined clock when in a normal mode of operation; and

a second scan controller having an input terminal connected to an output terminal of said first scan controller, for outputting a scan-out signal corresponding to a scan-in signal which is an input signal for testing the semiconductor integrated circuit device, in synchronism with said scan clock when the semiconductor integrated circuit device is tested.

2. A master-slave-type scanning flip-flop circuit according to claim 1, wherein said scanning flip-flop circuit comprises a D flip-flop circuit.

3. A master-slave-type scanning flip-flop circuit for use in testing a semiconductor integrated circuit device, comprising:

a master latch and a slave latch each for temporarily holding an input signal;

a clock controller for receiving an output signal from said master latch and outputting the received output signal to said slave unit in synchronism with a predetermined clock when in a normal mode of operation; and

a scan controller having an input terminal connected to an output terminal of said master latch, for outputting a scan-out signal corresponding to a scan-in signal which is an input signal for testing the semiconductor integrated circuit device, in synchronism with a scan clock which is a clock for testing the semiconductor integrated circuit device when the semiconductor integrated circuit device is tested.

4. A master-slave-type scanning flip-flop circuit according to claim 3, wherein said scanning flip-flop circuit comprises a J-K flip-flop circuit.

5. A master-slave-type scanning flip-flop circuit for use in testing a semiconductor integrated circuit device, comprising:

a master latch and a slave latch each for temporarily holding an input signal;

a clock controller for receiving an output signal from said master latch and outputting the received output signal to said slave unit in synchronism with a data signal supplied to the scanning flip-flop circuit when in a normal mode of operation; and

a scan controller having an input terminal connected to an output terminal of said master latch, for outputting a scan-out signal corresponding to a scan-in signal which is an input signal for testing the semiconductor integrated circuit device, in synchronism with a scan clock which is a clock for testing the semiconductor integrated circuit device when the semiconductor integrated circuit device is tested.

6. A master-slave-type scanning flip-flop circuit according to claim 5, wherein said scanning flip-flop circuit comprises a T flip-flop circuit.